Amendments to the Drawings:

The attached sheets of drawings replace the original sheets.

Attachment

Remarks/Arguments:

Claims 2-4 and 8-26 are pending. Claims 2-4 and 8-26 stand rejected.

Drawings:

Applicants have now submitted formal drawings as replacement sheets for the originally filed drawings.

The Office Action states that the "off-core and memory-mapped registers" must be shown or the features cancelled from the claims.

Applicants respectfully submit that these features are shown, for example, in FIGS. 4-6. Register 44 in FIG. 4 is referred to as "memory-mapped register 44", in the specification, at page 8, lines 15-16. Furthermore, the specification at page 7, lines 12-14, refers to the logic that performs memory-mapping and decodes an address to determine if the register is being accessed. This logic is shown in FIG. 6.

Moreover, the specification at page 7, lines 20-25, refers to FIG. 5 as including an "off-core register", in which the address and read-write decoding are unnecessary for off-core register operations. As shown in FIG. 5, for example, an "off-core register" includes a first set of 16 flip/flops 54 (as discussed at page 9, line 21).

Applicants respectfully submit that an off-core register and a memory-mapped register are shown in the figures.

Section 112 Rejections:

The Examiner has rejected claims 9, 14 and 20 as being indefinite because "it is not understood how a register can be coupled between two processors when a register, by definition, is a storage area located within the processor".

Applicants respectfully submit that although a processor likely includes registers, such registers may exist outside of the processor. Such architecture, for example, is supported by the discussion in the specification regarding the difference between an off-core register and a memory-mapped register.

As defined in the specification and shown, for example, in Figure 2, signal unit 23, which includes registers, is located between first processor 22 and second processor 24. As also shown in FIG. 4, for example, register 44 and edge detector 45 are both coupled between first processor 41 and second processor 46.

The Office Action also states that a register and an edge detector both coupled between the first and second processors is indefinite, because it is not made explicitly clear if there are one or two of such registers and etch detectors. Applicants have now amended claims 9, 14 and 20, so that each recites "at least one register and at least one detector" coupled between the first and second processors.

Applicants respectfully request that the Examiner reconsider these Section 112 rejections.

Section 103 Rejections:

Independent claims 9, 14 and 20 have been rejected as being obvious in view of Brown and Milton. Applicants respectfully submit that this rejection is overcome for the reasons set forth below.

Amended claim 9 now includes features which are not suggested by the cited references, namely:

- wherein the **active logic levels** stored in the register **are obtained from a single data word**, and
- **each of the interrupt signals corresponds to a respective active logic level of the single data word.**

Basis for amended claim 9 may be seen, for example, in FIG. 7 and is discussed in the specification at page 10, lines 10-25. As shown, data placed on the data bus includes a word of 16 bits. For each one of the 16 bits, a corresponding interrupt signal may be generated, as shown in FIG. 7(g). As further shown in FIGS. 7(h) and 7(i), as an example, two interrupts have been activated as interrupt (0) and interrupt (1). This is also discussed in the specification at page 11, lines 1-8.

In this manner, the invention uses **active bits from a single data word** as interrupt signals that may be routed from a first processor to interrupt terminals of a second processor. This advantageously reduces the number of dedicated output terminals required in the first processor, because the need for dedicated interrupt signal outputs is eliminated.

The Office Action states that Brown teaches a system for providing an interrupt signal including a data bus coupled to a first processor for routing parallel bits of data, a register and an edge detector coupled between the first and second processors. The Office Action admits, however, that Brown fails to teach providing an interrupt signal that is routed from a first processor to a second processor.

Moreover, Brown does **not** disclose that the **active logic levels stored in the register** are **obtained from a single data word**. Furthermore, Brown does **not** disclose that **each of the interrupt signals corresponds to a respective active logic level from the single data word**.

The Office Action states that Milton teaches a communication system between a digital signal processor and a main controller. The main controller controls the processor by using interrupt signals. Milton, however, does **not** disclose **active logic levels that are stored in a register in which the active logic levels have been obtained from a single data word**. Furthermore, Milton does **not** disclose that **each of the interrupt signals corresponds to a respective active logic level, which has been obtained from the single data word.**

Favorable reconsideration is requested for amended claim 9.

Although not the same, claims 14 and 20 have been amended to include features similar to amended claim 9. These claims are, therefore, not subject to rejection in view of the cited references for the same reasons set forth for amended claim 9.

Dependent claims 2-4, 8, 10-13, 15-19 and 21-26 depend from one of independent claims 9, 14 and 20. These dependent claims are, therefore, not subject to rejection in view of the cited references for at least the same reasons set forth for amended claim 1.

Conclusion

Claims 2-4 and 8-26 are in condition for allowance.

Respectfully submitted,

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Attachments: Figures 1-7 (5 sheets)

Dated: November 23, 2004

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The Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

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